

09/472865

15

348
2711

FIG. 1

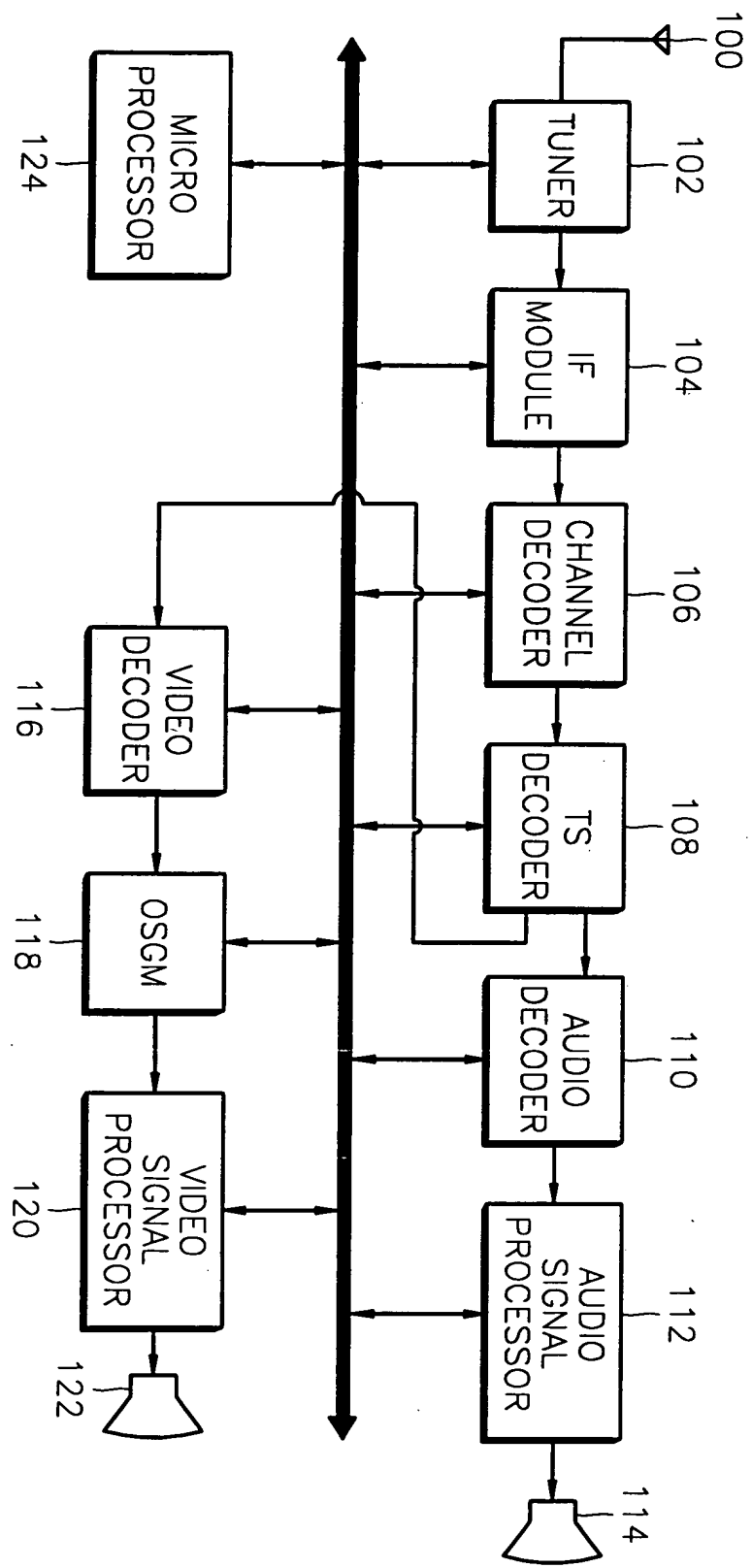
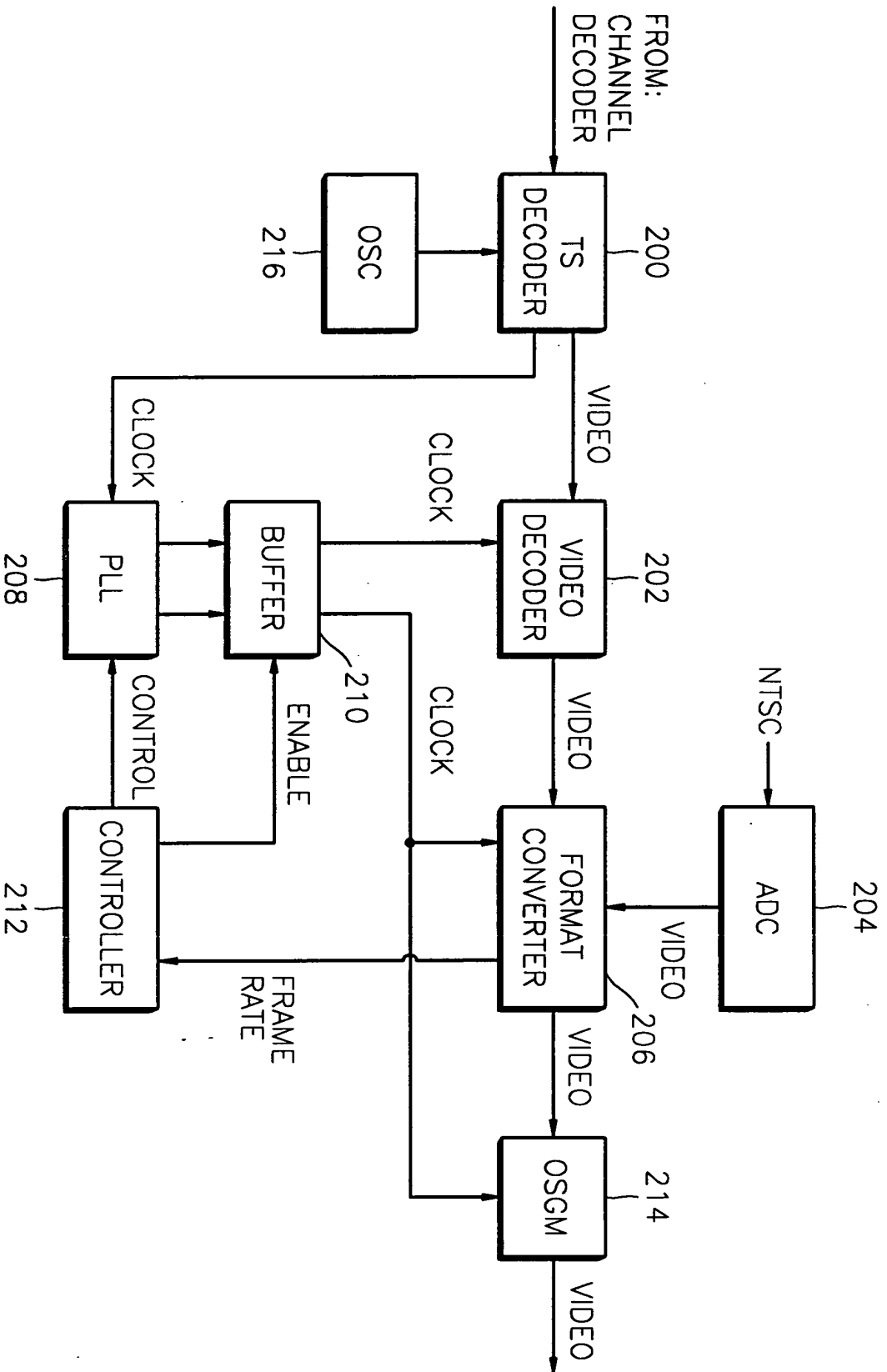


FIG. 1 is a block diagram of a video receiver system.

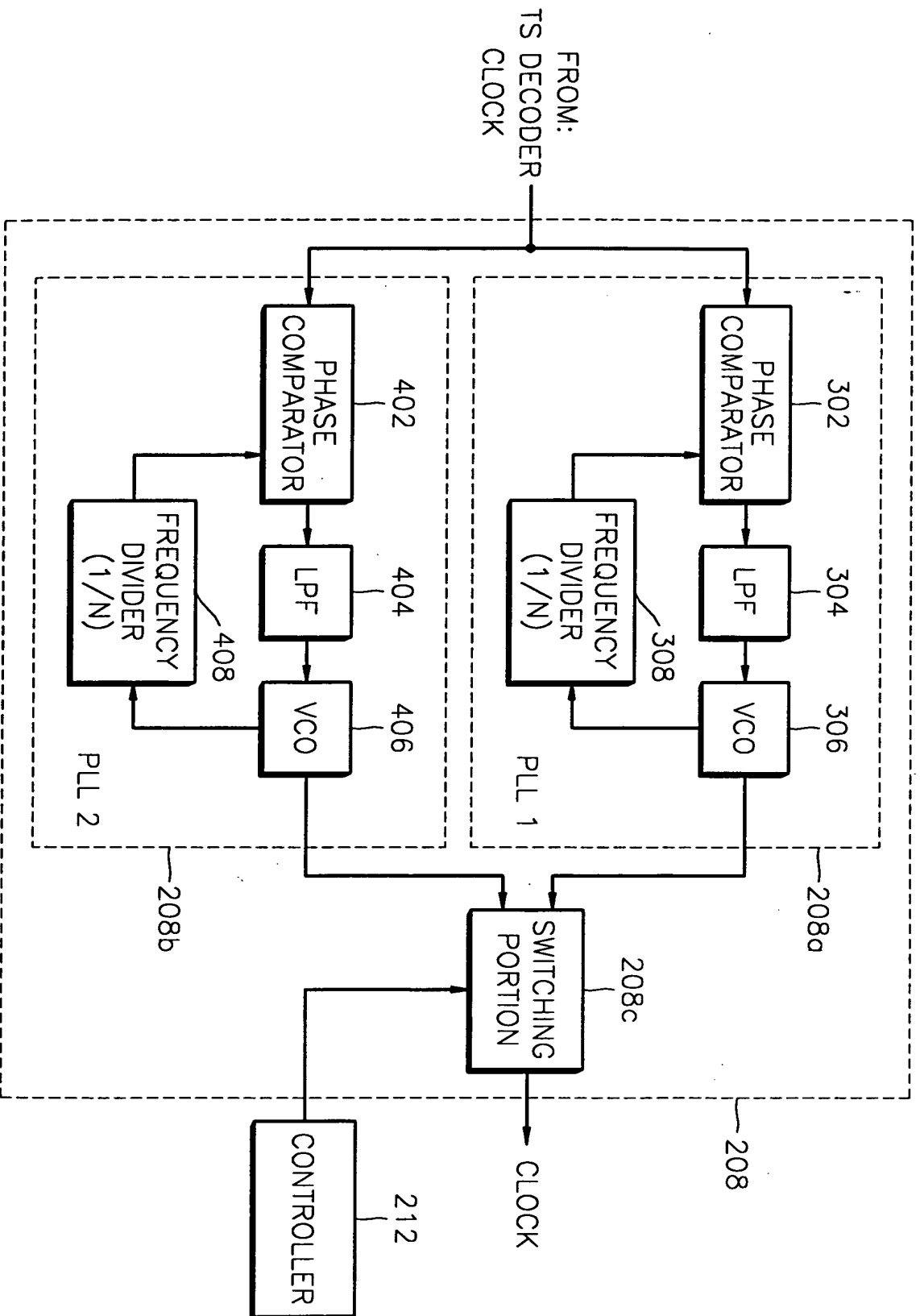
FIG. 2



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2008-09-29 14:23:29

FIG. 3



FROM:
TS DECODER
CLOCK

302

304

306

208a

208

208c

FREQUENCY
DIVIDER
(1/N)

PLL 1

CLOCK

402

404

406

212

PHASE
COMPARATOR

LPF

VCO

CONTROLLER

208b

FREQUENCY
DIVIDER
(1/N)

PLL 2